CLAIMS

1. (Currently amended) A system for processing an input signal, the system comprising:

[[-]]a predistortion subsystem adapted to receive said input signal and adapted to produce a predistorted signal by applying a deliberate predistortion to said input signal, wherein said predistortion subsystem is adapted to distort said input signal to compensate for distortions in a system output signal; and

[[-]]a signal processing subsystem adapted to receive and process said predistorted signal and adapted to produce ~~a~~ said system output signal, wherein said signal processing subsystem is adapted to decompose said predistorted signal into ~~separate~~ at least two components, each of said ~~separate~~ at least two components being processed separately~~;~~, ~~and~~ said signal processing subsystem ~~is~~ adapted to combine said at least two components after processing to produce said system output signal~~;~~, and wherein said signal processing subsystem comprises~~:~~

a signal decomposer adapted to decompose said predistorted signal into said at least two components, ~~each of the at least two components exhibiting a phase and a magnitude, the magnitude of at least two of the at least two components signals being substantially equal;~~

at least two signal component processor blocks, each of said at least two signal component processor blocks including ~~an~~ respective amplifier, each of said signal component processor blocks adapted to receive ~~an~~ respective one of said at least two components ~~output~~ from said signal decomposer, and each of said signal component processor blocks adapted to separately process said respective one of said at least two components and to produce a respective processed output ~~received from said signal decomposer;~~, and

a combiner adapted to receive ~~a~~ said respective processed outputs from each of said at least two signal component processor blocks, said combiner producing said system output signal from said respective processed outputs of said at least two signal component processor blocks;

wherein said predistorted signal is represented as a sequence of magnitude and phase pairs; and

wherein said signal decomposer includes a phasor fragmentation engine to receive said sequence of magnitude and phase pairs, said phasor fragmentation engine adapted to decompose said predistorted signal into said at least two components, each of said at least two components exhibiting a respective magnitude and having a respective varying phase, said respective magnitudes of at least two of said at least two components being substantially equal.

2. (Cancelled)

3. (Cancelled)

4. (Currently amended) ~~A~~ The system according to claim 1 wherein said respective amplifier comprises a non-linear amplifier.

5. (Currently amended) ~~A~~ The system according to claim 1 wherein said system is part of a signal transmission system.

6. (Currently amended) ~~A~~ The system according to claim 1 wherein at least some of said distortions are due to said combiner.

7. (Currently amended) ~~A~~ The system according to claim 1 wherein said respective amplifier comprises a switch mode amplifier.

8. (Currently amended) ~~A~~ The system according to claim 1 wherein said respective amplifier has a low-output impedance.

9. (Currently amended) ~~A~~ The system according to claim 1 wherein said deliberate predistortion includes magnitude distortions adapted to adjust a magnitude of said input signal.

10. (Currently amended) ~~A~~ The system according to claim 1 wherein said deliberate predistortion includes phase distortions adapted to adjust a phase of said input signal.

11. (Currently amended) ~~A~~ The system according to claim 1 wherein said deliberate predistortion is based on at least one entry in a lookup table.

12. (Currently amended) A method of processing an input signal to produce a system output signal, the method comprising:

receiving said input signal;

predistorting, via applying a deliberate predistortion, ~~to~~ said input signal to provide a predistorted signal represented as a sequence of magnitude and phase pairs;

decomposing said predistorted signal into at least two component signals~~; each of the at least two component signals exhibiting a phase and a magnitude, the magnitude of at least two of the said at least two component signals being substantially equal~~;

separately processing each of said at least two component signals, wherein said processing further includes amplifying each of said at least two component signals; and

combining said at least two component signals to produce said system output signal;

wherein said decomposing comprises receiving said sequence of magnitude and phase pairs and producing therefrom said at least two component signals, each of said at least two component signals exhibiting a respective magnitude and having a respective varying phase, said respective magnitudes of at least two of said at least two component signals being substantially equal.

13. (Currently amended) ~~A~~ The method according to claim 12 wherein said system output signal is an RF modulated version of said input signal.

14. (Cancelled)

15. (Cancelled)

16. (Currently amended) ~~A~~ The method according to claim 12 wherein said processing includes phase modulating at least one of said at least two component signals.

17. (Currently amended) ~~A~~ The method according to claim 12 wherein said receiving further includes accessing an entry in a lookup table, said deliberate predistortion being based, at least in part, on said entry.

18. (Currently amended) ~~A~~ The method according to claim 17 wherein said deliberate predistortion is based on an interpolation of entries in said table.

19. (Currently amended) ~~A~~ The system according to claim 11 wherein said deliberate predistortion is based on an interpolation of entries in said table.

20. (New) A system according to claim 1

wherein said phasor fragmentation engine is configured to convert said sequence of magnitude and phase pairs into two parallel sequences of phasors representing said at least two components, each of said phasors at a respective phase and substantially equal in magnitude to Vmax/2; and

wherein Vmax is a maximum amplitude of said predistorted signal over a period of said sequence of magnitude and phase pairs.

21. (New) A system according to claim 20

wherein said phasor fragmentation engine is adapted to determine the respective phases of a particular pair of said phasors derived from a particular one of said sequence of magnitude and phase pairs as $\theta-\varphi$ and $\theta+\varphi$ respectively; and

wherein V and θ are a respective magnitude and a respective phase of said particular one of said sequence of magnitude and phase pairs, and $\varphi=\cos^{-1}(V/Vmax)$.

22. (New) A system according to claim 1 wherein said respective amplifier comprises a class D amplifier.

23. (New) A method according to claim 12

wherein said decomposing comprises converting said sequence of magnitude and phase pairs into two parallel sequences of phasors representing said at least two component signals, each of said phasors at a respective phase and substantially equal in magnitude to Vmax/2; and

wherein Vmax is a maximum amplitude of said predistorted signal over a period of said sequence of magnitude and phase pairs.

24. (New) A method according to claim 23

wherein said decomposing determines the respective phases of a particular pair of said phasors derived from a particular one of said sequence of magnitude and phase pairs as $\theta-\varphi$ and $\theta+\varphi$ respectively; and

wherein V and θ are a respective magnitude and a respective phase of said particular one of said sequence of magnitude and phase pairs, and $\varphi=\cos^{-1}(V/Vmax)$.